PATENTS
ALT-155

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : Tony K. Ngai et al.

Application No.: 09/124,649

Filed : July 29, 1998

For : PROGRAMMABLE LOGIC DEVICE HAVING EMBEDDED DUAL-PORT RANDOM ACCESS MEMORY CONFIGURABLE AS SINGLE-PORT MEMORY

Group Art Unit : 2752

Examiner : Pierre-Michel Bataille

New York, New York 10020
October 20, 2000

Hon. Commissioner for Patents
Washington, D.C. 20231

SECOND SUPPLEMENTAL
INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants hereby make the following patents and publications of record in the above-identified patent application:

Kaplinsky U.S. Patent No. Re 34,444 (November 16, 1993)
Patil U.S. Patent No. 4,293,783 (October 6, 1981)
Carter U.S. Patent No. 4,642,487 (February 10, 1987)
Carter U.S. Patent No. 4,706,216 (November 10, 1987)
Carter U.S. Patent No. 4,758,985 (July 19, 1988)
Kawata U.S. Patent No. 4,825,414 (April 25, 1989)
Imazeki et al. U.S. Patent No. 4,831,591 (May 16, 1989)
Ikeda U.S. Patent No. 4,855,958 (August 8, 1989)
Freeman U.S. Patent No. 4,870,302 (September 26, 1989)
Nakayama et al. U.S. Patent No. 4,903,236 (February 20, 1990)
Keida U.S. Patent No. 4,963,770 (October 16, 1990)

Steele U.S. Patent No. 4,975,601 (December 4, 1990)
Agrawal et al U.S. Patent No. 5,042,004 (August 20, 1991)
Neal et al. U.S. Patent No. 5,089,993 (February 18, 1992)
Steele U.S. Patent No. 5,099,150 (March 24, 1992)
Chan et al. U.S. Patent No. 5,122,685 (June 16, 1992)
Steele U.S. Patent No. 5,128,559 (July 7, 1992)
Oh U.S. Patent No. 5,138,577 (August 11, 1992)
Steele U.S. Patent No. 5,144,582 (September 1, 1992)
Agrawal et al. U.S. Patent No. 5,212,652 (May 18, 1993)
Cliff et al. U.S. Patent No. 5,258,668 (November 2, 1993)
Pedersen et al. U.S. Patent No. 5,260,610 (November 9, 1993)
Cliff et al. U.S. Patent No. 5,260,611 (November 9, 1993)
Scott et al. U.S. Patent No. 5,291,444 (March 1, 1994)
Cooke et al. U.S. Patent No. 5,313,119 (May 17, 1994)
Snider U.S. Patent No. 5,315,178 (May 24, 1994)
Agrawal et al. U.S. Patent No. 5,329,460 (July 12, 1994)
Popli et al. U.S. Patent No. 5,336,950 (August 9, 1994)
Freeman et al. U.S. Patent No. 5,343,406 (August 30, 1994)
New U.S. Patent No. 5,349,250 (September 20, 1994)
Watson U.S. Patent No. 5,352,940 (October 4, 1994)
Stansfield U.S. Patent No. 5,408,434, (April 18, 1995)
Freidin U.S. Patent No. 5,414,377 (May 9, 1995)
Liu et al. U.S. Patent No. 5,425,036 (June 13, 1995)
Ong U.S. Patent No. 5,426,378 (June 20, 1995)
Pedersen et al. U.S. Patent No. 5,436,575 (July 25, 1995)
Huang U.S. Patent No. 5,448,522 (September 5, 1995)
Yumitori et al. U.S. Patent No. 5,471,425 (November 28, 1995)
Cliff et al. U.S. Patent No. 5,550,782 (August 27, 1996)
Freidin et al. U.S. Patent No. 5,566,123 (October 15, 1996)
Steele et al. U.S. Patent No. 5,809,281 (September 15, 1998)
Tsui et al. U.S. Patent No. 5,835,405 (November 10, 1998)
European Pat. Off. 0 081 917 (June 22, 1983)
European Pat. Off. 0 420 389 (April 3, 1991)

European Pat. Off. 0 415 542 (March 6, 1991)
European Pat. Off. 0 410 759 (January 30, 1991)
European Pat. Off. 0 507 507 (October 7, 1992)
European Pat. Off. 0 530 985 (March 10, 1993)
European Pat. Off. 0 569 137 (November 10, 1993)
Japan 1-91525 (April 11, 1989)
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PCT Int'l Appln. WO94/10754 (May 11, 1994)
PCT Int'l Appln. WO95/16993 (June 22, 1995)

"AT&T's Orthogonal ORCA Targets the FPGA Future," 8029 Electronic Engineering, 64, No. 786, June 1992, pp. 9-10

AT&T Microelectronics, "Optimized reconfigurable cell array (ORCA) series field-programmable gate arrays," pp. 1-87 (Advance Data Sheet, Feb. 1985)

Bursky, "Combination RAM/PLD Opens New Application Options," Electronic Design, May 23, 1991, pp. 138, 140

Bursky, D., "Denser, Faster FPGAs Vie for Gate-Array Applications," 2328 Electronic Design, 41, No. 11, May 27, 1993, pp. 55-75

Bursky, D., "FPGA Advances Cut Delays, Add Flexibility," 2328 Electronic Design, 40, No. 20, October 1, 1992, pp. 35-43

Bursky, D., "Shrink Systems with One-Chip Decoder, EPROM, and RAM," Electronic Design, July 28, 1988, pp. 91-94

Casselman, "Virtual Computing and The Virtual Computer," IEEE, July 1993, p. 43

Hsieh et al., "Third Generation Architecture Boosts Speed and Density of Field Programmable Gate Arrays," Proc. of IEEE CICC Conf., May 1990, pp. 31.2.1 to 31.2.7

Intel Preliminary Datasheet, "iFX780: 10ns FLEXlogic FPGA with SRAM Option," November 1993, pp. 2-24 through 2-46

Kautz, "Cellular Logic-in-Memory Arrays," IEEE Trans. on Computers, Vol. C-18, No. 8, Aug. 1969, pp. 719-27

Kawana, K. et al., "An Efficient Logic Block Interconnect Architecture for User-Reprogrammable Gate Array," IEEE 1990 Custom Integrated Circuits Conf., May 1990, CH2860-5/90/0000-0164, pp. 31.3.1 to 31.3.4

Landry, S., "Application-Specific ICs, Relying on RAM, Implement Almost Any Logic Function," Electronic Design, October 31, 1985, pp. 123-130

Larsson, T, "Programmable Logic Circuits: The Luxury Alternatives are Coming Soon," Elteknik-med-Aktuell

ElectroniK, No. 4, February 25-March 9, 1988, pp. 37-38, (with English abstract)

Ling et al., "WASMII: A Data Driven Computer on a Virtual Hardware," Proc. of IEEE Field Prog. Custom Computing Machines Conf., Napa, California, April 1993, pp. 33-42

Manning, "An Approach to Highly Integrated Computer Maintained Cellular Arrays," IEEE Trans. on Computers, Vol. C-26, No. 6, June 1977, pp. 536-52

Masumoto, R.T., "Configurable On-Chip RAM Incorporated into High Speed Logic Array," IEEE Custom Integrated Circuits Conference, Jun. 1985, CH2157-6/85/0000-0240, pp. 240-43

Ngai, Kai-Kit Tony, "An SRAM-Programmable Field-Reconfigurable Memory," Presentation at University of Toronto, Canada, June 1993, pp. 1-14

Patil et al., "A Programmable Logic Approach for VLSI," IEEE Trans. on Computers, Vol. C-28, No. 9, September 1979, pp. 594-601

Plus Logic "FPSL5110 Intelligent Data Buffer" Product Brief, Plus Logic, Inc., San Jose, California, October 1990, pp. 1-6

Quenot et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Proc. of IEEE FCCM Conf., Napa, California, February 1994, pp. 91-100

Quinnell, R.A., "FPGA Family Offers Speed, Density, On-Chip RAM, and Wide-Decode Logic," EDN, December 6, 1990, pp. 62, 64

Satoh, H. et al., "A 209K-Transistor ECL Gate Array with RAM," IEEE Jor. of Solid-State Circuits, Vol. 24, No. 5, October 1989, pp. 1275-79

Seitz, "Concurrent VLSI Architectures," IEEE Trans. on Computers, Vol. C-33, No. 12, Dec. 1984, pp. 1247-65

Shubat, A. et al., "A Family of User-Programmable Peripherals with a Functional Unit Architecture," IEEE Jor. of Solid-State Circuits, Vol. 27, No. 4, Apr. 1992, 0018-9200/92$03.00, pp. 515-29

Smith, D., "Intel's FLEXlogic FPGA Architecture," IEEE 1063-6390/93, 1993 pp. 378-384

Stone, "A Logic in Memory Computer," IEEE Trans. on Computers, Jan. 1970, pp. 73-78

Xilinx, Inc. The Programmable Logic Data Book, 1993

Xilinx, Inc., The Programmable Logic Data Book, pp. 2-5 through 2-102, 1994

Copies of the aforementioned patents and publications, which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

It is respectfully requested that these patents and publications be (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form PTO-1449, as considered and initialled by the Examiner, be returned with the next communication.

A check in the amount of $240.00, in payment of the fee set forth in 37 C.F.R. § 1.17(p), is enclosed herewith. The Director is hereby authorized to charge any additional fee that may be due, or credit any overpayment, in connection with this Second Supplemental Information Disclosure Statement, to Deposit Account No. 06-1075. A duplicate copy of this Second Supplemental Information Disclosure Statement is enclosed herewith.

An early and favorable action is respectfully requested.

Respectfully submitted,

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